Amendments to the Specification:

Please amend the paragraph beginning at page 9, line 14 as follows:

After the last delay output file has been created, the radius design cone delay output files and the global clock [[con]] cone delay output file are merged by the merge scripts 156 to produce a final SDF output file 158 in step 58. According to the present invention, the parallel delay prediction process 148 results in two benefits. One benefit is increased customer productivity. Due to partitioning and parallel processing, the parallel delay prediction process 148 requires only 4-6 hours to complete for a 10 million gate ASIC design, which is a significant improvement over the turnaround time for the monolithic approach. Another benefit is that the parallel delay prediction process 148 is scalable and predictable. That is, larger designs may be processed in the same amount of time by adding a proportionate number of computers. For example, delay prediction for a 20 million gate ASIC design may be processed in same time as a 10 million gate ASIC design by doubling the number of computers.